BUILT-IN CIRCUIT FOR SELF-TEST

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Abstract of **JP2001222900**

PROBLEM TO BE SOLVED: To obtain a built-in circuit for self-test in which increase of occupancy area in an integrated circuit can be suppressed by sharing a data generator generating a diagonal pattern even when RAMs having different shape are arranged in an integrated circuit.
SOLUTION: This circuit is provided with a X address register 2 composed of registers with up-counter generating X addresses of all RAMs performing a test and outputting them, a Y address register 3 composed of registers with up-counter generating Y addresses of all RAMs performing a test and outputting them, and a chip enable-control circuit section 4 generating an enable-signal from a X address and a Y address outputted from the X address register 2 and the Y address register 3 and outputting them to RAMs to be tested.